HARDWARE COMPLEXITY OF MICROPROCESSOR DESIGN ACCORDING TO MOORE'S LAW

Haissam El-Aawar

Associate Professor, Computer Science/Information Technology Departments
Lebanese International University – LIU, Bekaa – Lebanon
haisso@yahoo.com, haissam.aawar@liu.edu.lb

ABSTRACT

The increasing of the number of transistors on a chip, which plays the main role in improvement in the performance and increasing the speed of a microprocessor, causes rapidly increasing of microprocessor design complexity. Based on Moore's Law the number of transistors should be doubled every 24 months. The doubling of transistor count affects increasing of microprocessor design complexity, power dissipation, and cost of design effort.
This article presents a proposal to discuss the matter of scaling hardware complexity of a microprocessor design related to Moore's Law. Based on the discussion a hardware complexity measure is presented.

KEYWORDS

Hardware Complexity, Microprocessor Design, Transistor Count, Die Size, Density.

1. INTRODUCTION

Algorithms' Complexity is regarded as one of the significant measurement, which is appearing along the recent past. Although, there is a rapid development in the algorithmic devices, which involve a computer system as one of their examples; complexity is still occupying a major role in computer design, if it is thought to be oriented towards the hardware or software view [1, 2].
The development of IC technology and design has been characterized by Moore's Law during the past fifty years. Moore's Law states that the transistor count on a chip would double every two years [3, 4]; applying Moore's law in the design of the microprocessors makes it more complicated and more expensive. To fit more transistors on a chip, the size of the chip must be increasing and/or the size of the transistors must be decreasing. As the feature size on the chip goes down, the number of transistors rises and the design complexity also rises.

Microprocessor design has been developed by taking into consideration the following characteristics: performance, speed, design time, design complexity, feature size, die area and others. These characteristics are generally interdependent. Increasing the number of transistors raises the die size, the speed and the performance of a microprocessor; more transistors, more clock cycles. Decreasing the feature size increases the transistor count, the design complexity and the power dissipation [5, 6].

Natarajan Meghanathan et al. (Eds) : ICAIT, ICDIPV, ITCSE, NC - 2014
pp. 01–07, 2014. © CS & IT-CSCP 2014 DOI : 10.5121/csit.2014.4701

2. HARDWARE COMPLEXITY MEASUREMENT

Hardware complexity measurement is used to scale the number of elements, which are compounded, along any selected level of hardware processing. Any selected level, includes all the involved structures of hardware appearing beyond a specific apparatus. The hardware complexity measurement id defined as:

$$A = | E | \qquad (1)$$

where, E is the multitude of the elements emerging in a hierarchal structural diagram.

In order to illustrate when a processor level is selected (see Figure.1), the apparatus complexity measure (ACM) would be defined by the amount of the beyond registers, ALU and the Control Unit.

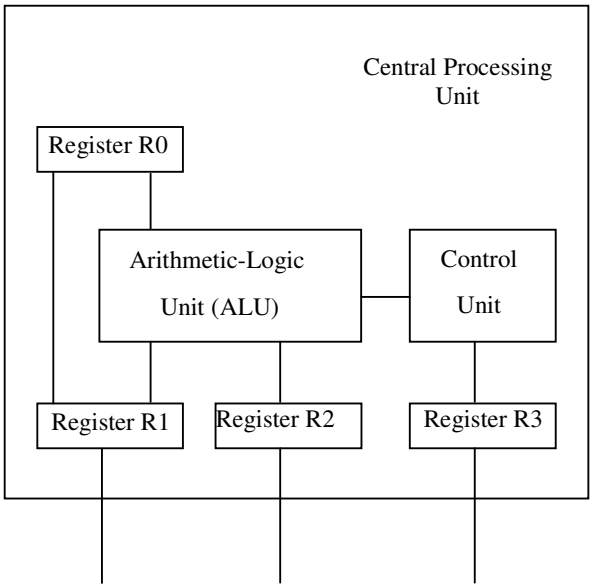

Figure.1.View of a CPU complexity Level, [7].

For the given example of Figure.1: ACM = | E | = 6.
So, the increasing of the number of elements at any processor level increases the hardware complexity of that level.

3. PHYSICAL LIMITATION OF INCREASING THE NUMBER OF TRANSISTORS

Increasing the number of transistors will be limited due to several limitations, such as increasing the density, the die size, decreasing the feature size, the voltage [8, 9, 10].

Since the surface area of a transistor determines the transistor count per square millimeter of silicon, the transistors density increases quadratically with a linear decrease in feature size [11]. The increase in transistor performance is more complicated. As the feature sizes shrink, devices shrink quadratically in the horizontal and vertical dimensions. A reduction in operating voltage to maintain correct operation and reliability of the transistor is required in the vertical dimension

shrink. This combination of scaling factors leads to a complex interrelationship between the transistor performance and the process feature size.

Due to the shrinking of the pixel size and the increasing of the density, the hardware complexity raises. If the pixel size shrinks double and the density increases double every two years according to Moore's Law, the physical limitation will definitely appear in few years, which means that it will be very difficult to apply Moore's Law in the future. Some studies have shown that physical limitations could be reached by 2018 [12] or 2020-2022[13, 14, 15, 16].

Applying Moore's Law by doubling the number of transistors every two years increases the speed and performance of the processor and causes increasing the processor's hardware complexity (see Table 1), which will be limited after a few years [17, 18, 19, 20].

Table 1. Complexity Of microchip And Moore's Law

Year	**Microchip Complexly Transistors**	**Moore's Law: Complexity: Transistors**
1959	1	$2^0 = 1$
1964	32	$2^5 = 32$
1965	64	$2^6 = 64$
1975	64,000	$2^{16} = 64{,}000$

Table 2 shows the apparatus complexity measurement of different microprocessors from 1971 till 2012.

Table 2. Evolution of Microprocessors And Apparatus Complexity Measurement: 1971 to 2012

Manufacturer	**Processor**	**Date of introduction**	**Number of transistors (Apparatus Complexity)**	**Area [mm^2]**
Intel	Intel4004	1971	2,300	12
	Intel8008	1972	3,500	14
	Intel8080	1974	4,400	20
	Intel8085	1976	6,500	20
	Intel8086	1978	29,000	33
	Intel80286	1982	134,000	44
	Intel80386	1985	275,000	104
	Intel80486	1989	1,180,235	173
	Pentium	1993	3,100,000	294
	Pentium Pro	1995	5,500,000	307
	Pentium II	1997	7,500,000	195
	Pentium III	1999	9,500,000	128
	Pentium 4	2000	42,000,000	217
	Itanium 2 McKinely	2002	220,000,000	421

	Core 2 Duo	2006	291,000,000	143
	Core i7 (Quad)	2008	731,000,000	263
	Six-Core Core i7	2010	1,170,000,000	240
	Six-Core Core i7/8-Core Xeon E5	2011	2,270,000,000	434
	8-Core Itanium Poulson	2012	3,100,000,000	544
MIPS	R2000	1986	110,000	80
	R3000	1988	150,000	56
	R4000	1991	1,200,000	213
	R10000	1994	2,600,000	299
	R10000	1996	6,800,000	299
	R12000	1998	7,1500,000	229
IBM	POWER3	1998	15,000,000	270
	POWER4	2001	174,000,000	412
	POWER4+	2002	184,000,000	267
	POWER5	2004	276,000,000	389
	POWER5+	2005	276,000,000	243
	POWER6+	2009	790,000,000	341
	POWER7	2010	1,200,000,000	567
	POWER7+	2012	2,100,000,000	567

4. INCREASING THE DIE SIZE

This article suggests, as a solution for avoiding the physical limitations mentioned above, a new approach of constructing a chip with die size that contains free spaces for allowing to apply the Moore's Law for a few years by doubling the number of transistors on a chip without touching the voltage, the feature size and the density, in this case only the hardware complexity will be raised.

Let us assume a microprocessor (let's say X) has the following specifications: date of introduction – 2015, one-layer crystal square of transistors, transistor count (number of transistors) – 3 billion, pixel size (feature size) – 0.038 micron, die size (area) – 2400 mm2: for transistors – 600 mm2 and free space – 1800 mm2 (see Figure. 2).

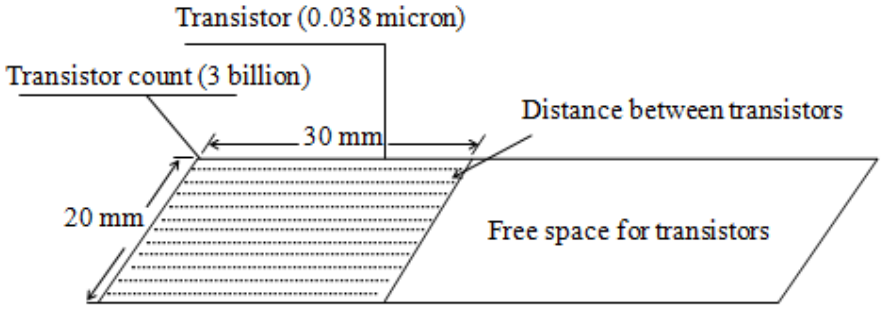

Figure 2. Crystal Square of Transistors

In this case the number of transistors will be doubled after two year (2017) without touching the feature size, die size, voltage and density. In 2017 year a new microprocessor (let's say X1) will have the following specifications: date of introduction – 2017, one-layer crystal square of transistors, transistor count (number of transistors) – 6 billion, pixel size (feature size) – 0.038 micron, die size (area) – 2400 mm^2: for transistors – 1200 mm^2 and free space – 1200 mm^2 and so on. When the number of transistors would occupied all the free space, the architects can decrease the feature size and increase the density without touching the die size (see Table 3).

Table 3. Assuming Evolution Of Microprocessors: 2015 to 2021

Microprocessor	**Date of introduction**	**Number of transistors (billion)**	**Feature size (nm)**	**Area [mm^2]**	
				For Transistors	**Free space**
X	2015	3	38	2400	
				600	1800
X1	2017	6	38	1200	
				1200	1200
X2	2019	12	38	2400	
				2400	
X3	2021	24	28	2400	

As shown in the table above, several measures of microprocessors technology, such as hardware complexity can be changed (increased) during few years, while the others can be fixed.

5. CONCLUSION

The problem of applying Moore's law in microprocessor technology as much as possible is still topical research field although it has been studied by the research community for many decades. The main objective of this article is to find a suitable solution for avoiding physical limitation in manufacturing of microprocessors technology and applying Moore's Law for a long time.

As mentioned above, the physical limitations could be reached by 2018 or 2022. Applying the new approach in microprocessor technology will delay the physical limitation for few more years, because it doubles the transistor count every two years based on Moore's Law, with increasing the die size and the hardware complexity, without decreasing of the feature size and increasing of the density.

ACKNOWLEDGMENT

The author would like to thank the president of Lebanese International University HE Abdel Rahim Mourad and the LIU Bekaa campus administration for their continuous encouragement of research activities at the university.

REFERENCES

[1] Cherkaskyy M. V. and Haissam El-Aawar, "Optimization of Complexity of Software/Hardware of Microprocessor Level", Proceedings of CAD essentials, implementation and Applications Symposium", Vol: 2, p: 200-201, 1997, Ukraine.

[2] Haissam El-Aawar; "Theory of Complexity of Algorithmic Devices", Proceedings of the 14th International Conference on Computer Theory and Applications ICCTA' 2004. Alexandria, Egypt, 2004.

[3] Gorden E. Moore, "cramming more Components onto Integrated Circuits", Electronics, Vol. 38, No. 8, April 19, 1965.

[4] Jane Laudon, Kenneth Laudon, "Essentials of Management Information Systems", Chapter 4: IT Infrastructure: Hardware and Software, 10th ed., 2012.

[5] Steve Gilheany, "Evolution of Intel Microprocessors: 1971 to 2007". http:// www.iro.umontreal.ca / ~aboulham/F2880/EvolutionMicroprocessor1971a2007.

[6] Wolfgang Arden, "Future roadblocks and solutions in silicon technology as outlined by the ITRS roadmap" in Mterials Science in Semiconductor Processing, vol. 5 issue 4-5 August – October, 2002, pp. 313-319.

[7] John P. Hayes, " Digital System Design and Microprocessors", McGraw-Hill press. 1987, USA.

[8] Hasan S., Humaria, Asghar M., "Limitation of Silicon Based Computation abd Future Prospects" in Proceedings of Second International Conference on Communication Software and Networks, 2010. ICCSN'10, pp. 599-561.

[9] Robert W. Keyes, "Physical limits of silicon transistors and circuits", September 2005.

[10] F. Morals, L. Torres, M. Robert, D. Auvergne, "Estimation of layout densities for CMOS digital circuits", Proceeding International Workshop on Power and Timing Modeling Optimization Simulation (PATMOS'98), pp. 61-70, November 1998, Lyngby, Danemark.

[11] John L. Hennessy and David A. Patterson, "Computer Architecture, A Quantitative Approach", 5th ed., pp. 17-26, 2011.

[12] Jan M. Rabaey, "Design at the end of Silicon Roadmap", Keynotes Address III, University of California, Berkelev, IEEE, ASP-DAC 2005.

[13] Ahmad, Khaled; Schuegraf, Klaus, "Transistor Wars: Rival architecture face off in a bid to keep Moore's Law alive", IEEE Spectrum: 50, November 2011.

[14] Brooke Crothers, "End of Moore's Law: it's not just about physics", August 28, 2013.

[15] Robert Colwell, "The Chip Design Game at the End of Moore's Law", Hot Chips, August 2013. http://news.cnet.com/8301-1001_3-57600373-92/end-of-moores-law-its-not-just-about-physics/

[16] Joel Hruska, "Intel's former chief architect: Moore's law will be dead within a decade", August 30, 2013. http://www.extremetech.com/computing/165331-intels-former-chief-architect-moores-law-will-be-dead-within-a-decade.

[17] Mike Stojcev, Teufic Tokic and Ivan Milentijevic, "The Limits of Semiconductor Technology and Oncoming Challenges in computer Microarchitectures and Architectures", Ser.: Elec.Energ. vol. 17, December 2004, pp. 285-312.

[18] Suleiman Abu Kharmeh, Kerstin Eder, and David May. Complexity of Hardware Design and Model-Checking: An Asymptotic Analysis of State-Machine Metrics. Technical report, University of Bristol, March 2012.

[19] Cyrus Bazeghi, Francisco J. Mesa-martinez, Brian Greskamp , Josep Torrellas, Jose Renau, "μComplexity: Estimating Processor Design Effort", International Symposium on Microarchitecture, 2005.

[20] Pradip Bose David H. Albonesi Diana Marculescu, "Complexity-Effective Design", Proceeding International Workshop on Complexity-Effective Design, Madison, Wisconsin, June 5, 2005.

AUTHOR

Haissam El-Aawar is an Associate Professor in the Department of Computer Science and Information Technology at the Lebanese International University where he has been a faculty member since 2009. Haissam completed his Ph.D. and M.Sc. degrees at the State University "Lviv Polytechnic" in Ukraine. His research interests lie in the area of Artificial Intelligence, theory of complexity, microprocessors evaluation, CISC- and RISC-architectures, robotics control, mobility control and wireless communication.