Capacitance-voltage Profiling Techniques for Characterization of Semiconductor Materials and Devices

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Abstract

A new capacitance-voltage profiling technique of semiconductor junctions is proposed for characterisation of semiconductor materials and devices. The measurement technique is simple, non-destructive and it has a greater accuracy compared with the classical C-V method of J. Hilibrand and R. D. Gold, developed in 1960.

Keywords

Capacitance-voltage, Profiling Technique, Semiconductor Junctions, Materials & Devices

1. Introduction

In 1960, a formula was found by J. Hilibrand and R. D. Gold to measure the impurity/doping profiles by means of capacitance-voltage measurements [1]. Their method was included in reference books authored by well-known authors like A.S. Grove [2], Simon Sze [3] and others. This measurement method involves reverse biasing the junction with a sweeping bias (V_R) and getting the barrier capacitance (C_b). From $C(V_R)$ data then N(x) is inferred – N being the doping concentration, usually measured in cm^{-3} and x is the spatial coordinate (cm or μm). The method is widespread, but over the years, researchers and semiconductor industry professionals found discrepancies between the $C_b(V_R)$ obtained data and actual doping profiles.

2. Advantages of the C-V technique

Compared with other semiconductor profiling techniques (spreading resistance, differential conductance, Hall effect, SIMS, RBS etc.), the C-V method is an electric, non-destructive measurement of the barrier capacitance of semiconductor junctions, like p-n junctions, metal-semiconductor junctions and even metal-oxide-semiconductor (MOS) structures. This non-destructive character and large applicability gave the method a widespread, almost universal usage in the semiconductor industry.

3. The theory of Hilibrand and Gold C-V formula

3.1. Doping profile versus electric charge density

The C-V (capacitance versus voltage) measurement is performed on an asymmetric semiconductor junction, a p^+n junction for example (Figure 1). The junction is formed at Xj = 0

coordinate where the concentrations of acceptors from the p^+ side equals the concentration of donors from the n side.

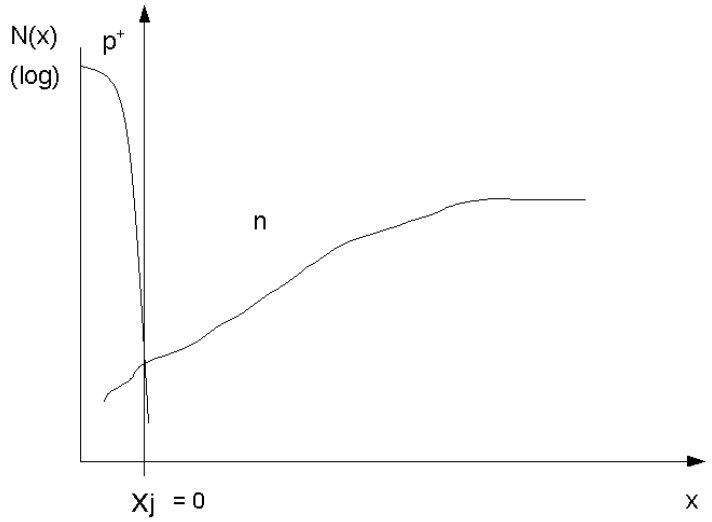

Figure 1. The concentrations of impurities in a p^+n junction (asymmetric type)

At the application of reverse biased, the space-charge region of the junction spreads mainly in the low doped side (n in this case). Hilibrand and Gold used the depletion-approximation, so the electric charge distribution is depicted in Figure 2.

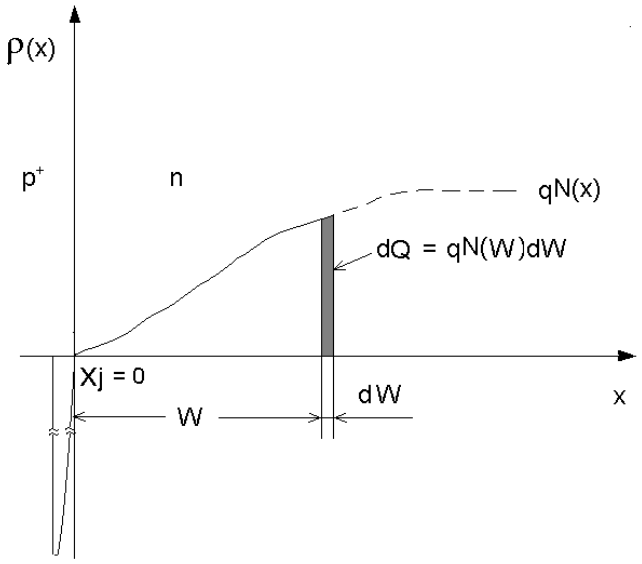

Figure 2. The depletion approximation for the charge distribution in an asymmetric p^+n junction

By neglecting the widening of the space-charge region in the heavily-doped side of the junction, it is obtained that W is equal to the SCR width. Then it is measured the barrier capacitance, knowing the formula:

$$C=\varepsilon/W \quad (1)$$

where ε is the permittivity of the semiconductor material (C expressed in F/cm^{-2}, usually).
Because

$$C=dQ/dV \quad (2)$$

and from (Figure 2)

$$dQ=qN(W)dW \quad (3)$$

from (1)

$$dW = d(\varepsilon C^{-1})=- \varepsilon C^{-2}dC \quad (4)$$

also from (2) and (3)

$$dV=dQ/C=-qN(W)\ \varepsilon C^{-2}dC/C \quad (5)$$

Now results the doping concentration at the current coordinate (W in Figure 2) as:

$$N(W)=-(C^3/q\varepsilon)/(dC/dV) \quad (6)$$

or

$$N(W)=(2/q\varepsilon)/[d(1/C^2)/dV] \quad (7)$$

This is the formula deduced by Hilibrand and Gold.

An example of measuring the bulk doping concentration of a silicon sample is given in Figure 3. Calculating the slope of $(1/C^2)$ versus voltage graph, the bulk concentration N_B is found, since for a uniformly doped semiconductor [2]:

$$1/C^2 = 2(V_R + V_{bi})/q\varepsilon N_B \quad (8)$$

Also, the value of the built-in voltage V_{bi} of the junction is found at the intersection of the $(1/C^2)$ line with the horizontal axis. From Figure 3 and eq.(8), $1/C^2 = 0$ when $V = -V_R = V_{bi}$.
A more precise measuring will take into account 2kT/q (about 50 mV) to be added to the obtained value of V_{bi} [4], but since V_{bi} is around 700 mV this correction is negligible (k is the Boltzmann constant and T the absolute temperature).

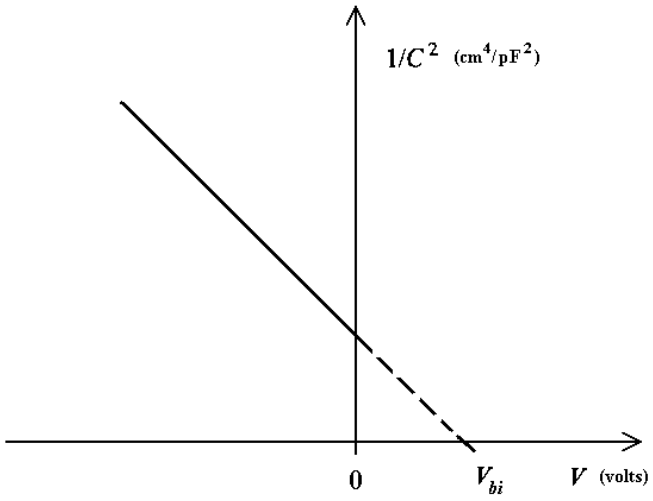

Figure 3. $1/C^2$ plot of the barrier capacitance used to determine the background concentration N_B and built-in potential V_{bi} of a semiconductor junction

3.2. Flaws of the classic formula

Over the years, researchers in the semiconductor industry found discrepancies between the C-V formula results and actual doping profiles. They also found inaccuracies near the junction due to the fact that, when the doping profile abruptly changes in a scale smaller than the Debye length L_D, the analysis is no longer valid because the profile variation cannot be resolved [4].
So they developed various reverse engineering and iterative methods to overcome them, including flow-charts, to near the experimental results with the actual doping profile [5, 6].
The main discrepancies are caused by the limited validity of the depletion approximation at the edge of the depletion zone. Actually, in formula (3) appears the net concentration N(W)-n(W) and not the doping concentration N(W), where n(W) is the mobile carrier concentration (electrons), neglected in the depletion approximation (Figure 4). From this figure it is clear that the targeted doping concentration N(W) is 2-3 times or even higher than the measured value N(W)-n(W).

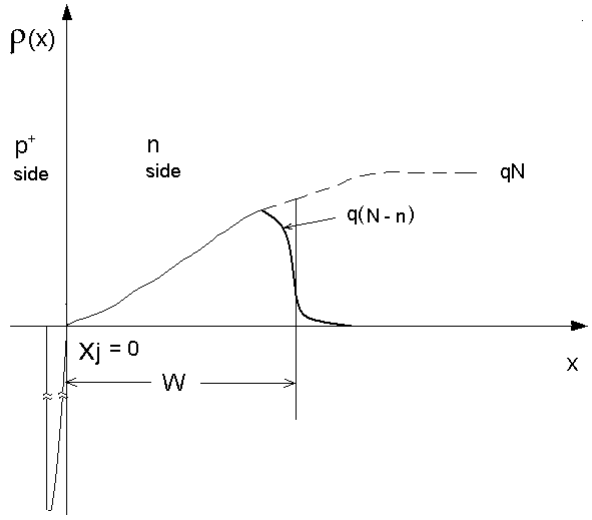

Figure 4. The real case of an asymmetric p^+n junction charge distribution

4. Deduction of a new, correct formula

4.1. A new formula of physics

In this section a new formula is deduced from the Gauss' Law and the electric field (E)/ electric potential (V) relation. From these two formulas was deduced also the well-known Poisson equation. Nevertheless, this is an entirely new formula, able of solving problems that Poisson equation couldn't solve, as shown below.

The differential form of Gauss' Law shows the connection between the electric field and the electric charge density:

$$dE/dx = \rho(x)/\varepsilon \qquad (9)$$

This holds for any linear material or space region where ε does not depend on the electric field intensity.

The potential V versus the electric field E is given by:

$$E = - dV/dx \qquad (10)$$

Writing (9) as

$$dE = \rho(x)dx/\varepsilon \qquad (11)$$

then performing a multiplication with x and considering that

$$d(xE) = xdE + Edx \qquad (12)$$

the integrable formula is obtained:

$$d(xE) - Edx = x\rho(x)dx/\varepsilon \qquad (13)$$

The integration of (13) over the space charge region defined between coordinates X1 and X2 gives

$$\int_{X1}^{X2} \frac{x\rho(x)}{\varepsilon} dx = \int_{X1}^{X2} d(xE) - \int_{X1}^{X2} E dx \tag{14}$$

and taking (10) into account, then

$$\int_{X1}^{X2} \frac{x\rho(x)}{\varepsilon} dx = \int_{X1}^{X2} d(xE) + \int_{X1}^{X2} dV \tag{15}$$

Both terms in the right hand of this equation are perfect integrals. The right side results, by integration:

$$\int_{X1}^{X2} \frac{x\rho(x)}{\varepsilon} dx = V(x_2) - V(x_1) + x_2 E(x_2) - x_1 E(x_1) \tag{16}$$

The applicability of this new equation is not limited to semiconductor junctions, but it extends in the electro-magnetic field theory [7].

4.2. Application to semiconductor junctions

Since the electric field is zero at both ends of the SCR [8], particularization of (16) to semiconductor junctions leads to

$$\int_{SCR} \frac{x\rho(x)}{\varepsilon} dx = V_{bi} - V_F \tag{17}$$

where V_{bi} is the built-in voltage of the junction and V_F is the externally applied forward bias. If the junction is subjected to reverse bias, V_F should be replaced with $-V_R$, therefore equation (17) becomes:

$$\int_{SCR} \frac{x\rho(x)}{\varepsilon} dx = V_{bi} + V_R \tag{18}$$

In the case of homogenous semiconductor junctions, this formula can be written as:

$$\frac{1}{\varepsilon} \int_{SCR} x\rho(x) dx = V_{bi} + V_R \tag{19}$$

since the permittivity is constant throughout the material.

However, in the case of hetero-junctions or other types of junctions in which more than one material is encountered, the following form of equation (18) should be applied:

$$\int_{SCR1} \frac{x\rho(x)}{\varepsilon_1} dx + \int_{SCR2} \frac{x\rho(x)}{\varepsilon_2} dx + \ldots + \int_{SCRn} \frac{x\rho(x)}{\varepsilon_n} dx = V_{bi} + V_R \tag{20}$$

where SCR1, SCR2... SCRn are the fractions of the overall space charge region corresponding to the n semiconductor materials used for the junction fabrication.
Equation (19) can also be used in the next format when the device has a particular geometry:

$$\frac{1}{\varepsilon} \int_{SCR} (x + k_x)\rho(x)\, dx = V_{bi} + V_R \tag{21}$$

where k_x is a constant distance. This equation can be deduced following the algorithm used for (16), or by noticing that

$$\frac{k_x}{\varepsilon} \int_{SCR} \rho(x)\, dx = 0 \tag{22}$$

due to the space charge equilibrium law for the electric charge on both sides of the junction.

5. The new C-V measurement technique

5.1. Practical example

In Figure 5 is depicted the doping profile of the base-emitter junction of a bipolar transistor showing the extension of the space charge region (SCR) occurring mostly in the lightly-doped side of the junction (base).

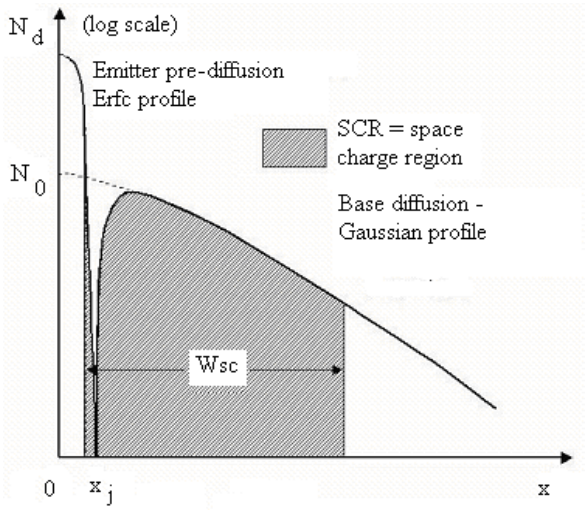

Figure 5. Base-emitter junction doping profile and space charge region (SCR) of a bipolar transistor with diffused base

Supposing that the base-emitter junction is reverse-biased, we obtain by the integration of equation (18) the formula of the barrier capacitance of the junction [7]:

$$C_b = \frac{\varepsilon}{L_d \left\{ \sqrt{-\ln\left[e^{-\frac{x_j^2}{L_d^2}} - \frac{2\varepsilon}{qN_0 L_d^2}(V_R + V_{bi}) \right]} \right\} - x_j} \tag{23}$$

Above, x_j is the junction depth, N_0 is the surface concentration of the Gaussian diffusion and Ld is the technological diffusion length of the doping impurities $L_d = 2\sqrt{D_i t_d}$, with Di the diffusion constant of the impurities and t_d their diffusion time during the fabrication of the p-n junction. Other particular cases derived from (23) were analyzed in [7].

5.2. Experimental results for Gaussian-type junctions

Semiconductor devices such as bipolar transistors, thyristors, IGBTs and other devices with diffused base share the same doping profile as depicted in Figure 5 [7, 9]. For these devices, and also for p-n diodes, varicap diodes and other semiconductor devices, it is of interest to find the parameters of the diffused base using a non-invasive, non-destructive technique [10], like the C-V measurement of the barrier capacitance of the p-n junction. We measured the barrier capacitance C_B at various reverse voltage values.

$$C_B = A_J C_b \tag{24}$$

Here C_b is the specific capacitance and A_J is the junction area.

The measurements were made with a KEITHLEY C-V ANALYZER 590 Semiconductor Characterisation System using its sine voltage 15 mV rms test signal. The frequency of 100kHz was used for the C-V measurements because it has better accuracy then 1MHz test frequency (0.12% vs. 0.29%). A 1MHz test frequency is traditionally specified in C-V test procedures requiring high-frequency device characteristics. The measurement circuit is very simple using the transistor connected with the emitter-base terminals at the measurement input and the collector decupled with 100 nF capacitor to the ground of the C-V analyser.

From the $C(V_R)$ experimental curve connected with equations (23) and (24), the parameters of bipolar transistor types like BD 235 and BF307 were extracted with the aid of curve-fitting programs like EasyPlot or MathCAD [10]. The extracted parameters are - from eqns. (23) and (24): A_J – the junction area, N_0 – the surface concentration of the diffusion, L_d – the technological diffusion length and V_{bi} – the built-in junction potential. The obtained parameters were in good agreement with the known device layouts and technological process data like the total diffusion time.

6. Proposal

Although widely used for almost 50 years, the C-V doping profiling formula of Hilibrand and Gold from 1960 proved to be flawed. The main flaws are the facts that it doesn't measure the doping but rather the net electric charge concentration at the space-charge region boundary and that it cannot follow steep variations of the doping profile.
Based on a new physics formula discovered in 2006, a new C-V parameter extraction technique was established and applied to semiconductor junctions. Once a suitable analytical model is established for the doping profile, this new method extracts the parameters of that model by integration over the entire space-charge region; therefore it is not very much influenced by the errors occurring at the space-charge region boundaries.
The proposal is to apply this new C-V measurement technique to all doping profiles of semiconductor junctions since it has a better theoretical foundation. The measurement technique can be done with very simple laboratory instrumentation, like a DC power supply, a 1-10 MHz signal generator, an oscilloscope, but it can also benefit from specialized characterisation systems, like e.g. the KEITHLEY C-V ANALYZER 590 Semiconductor Characterisation System.

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